AMENDMENTS TO THE CLAIMS

E1 cont

1. (currently amended) A CMOS image sensor circuit, comprising:

a first CMOS image sensor chip including a substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and a control portion with image sensor logic on said substrate, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually, said image sensor portion having a first area and a second area;

said ~~image sensor~~ substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge;

said image sensor ~~substrate~~ portion including imaging pixels extending between said first edge, said second edge, and said third edge, such that pixels of said first area of said image sensor portion ~~is~~ are adjacent said first edge and said third edge of said ~~image sensor~~ substrate and pixels of said second area of said image sensor portion ~~is~~ are adjacent said second edge and said third edge of said ~~image sensor~~ substrate;

said row logic being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion;

a pixel interpolator and said chip driver circuitry located between said first area and said second area of said image sensor portion and said fourth edge of said ~~image sensor~~ substrate; and

a second CMOS image sensor chip ~~substrate~~ configured similarly to said first CMOS image sensor chip ~~substrate~~ and abutted to one of said substrate edges of said first CMOS image sensor ~~substrate~~ chip.

E' Cont

2. (previously presented) A circuit as in claim 1 wherein said row logic is formed in place of two columns of the array forming the image sensor portion.

3. (currently amended) A circuit as in claim 1 wherein said image sensor portion extends within two pixel pitches of said first, second, and third edges of the ~~chip~~ substrate.

4. (original) A circuit as in claim 3 wherein said first and second edges are perpendicular to said third and fourth edges.

5. (currently amended) A circuit as in claim 1 ~~further comprising an~~ wherein said pixel interpolater operates ~~interpolating element, operating~~ to interpolate pixels which would have been active in areas of said image sensor portions taken up by said row logic and by space between said CMOS image sensor ~~substrates~~ portions.

6. (previously presented) A circuit as in claim 1 wherein said row logic is in the center of the plurality of pixels forming the image sensor portion.

7. (previously presented) A circuit as in claim 1 wherein the ends of the image sensor portion include a guard ring.

E1 Cont

8. (currently amended) A method of operating a large format image sensor, comprising:

first obtaining an image sensor chip which has first and second edges ~~where said~~ and an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edges, and includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array~~, and an image portion divided into two areas~~;

abutting said image sensor chip against a similar image sensor chip of corresponding construction; and

interpolating missing pixels on chip, the missing pixels being caused by both said row select logic and by spaces between said image sensor chips.

9. (previously presented) A CMOS imager, comprising:

a first CMOS image sensor having an image sensor portion arranged in an array of rows and columns, said first CMOS image sensor formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge; and

said first CMOS image sensor having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located

inside said image sensor portion in place of a plurality of pixels of the array forming said CMOS image sensor portion and thereby forming at least two image sensor areas, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said first CMOS image sensor.

E1 Cont

10. (original) The CMOS imager according to claim 9, further comprising a second CMOS image sensor configured similarly to said first CMOS image sensor and abutted to one of said edges of said first CMOS image sensor.

11. (currently amended) A method of fabricating a CMOS imager comprising:

fabricating at least two CMOS image sensors having an image sensor portion arranged in an array of rows and columns, each of said at least two CMOS image sensors formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge, said at least two image sensors each having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor and thereby forming at least two image sensor areas for each of said at least two CMOS image sensors, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said image sensor;

abutting said at least two CMOS image sensors together; and

integrating said control portions of said at least two CMOS image sensors such that said at least two CMOS image sensors function as a single CMOS imager.

E1 cont

12. (previously presented) The method of fabricating according to claim 11, further comprising interpolating, using said pixel interpolator of said control portion, missing pixels caused by said centralized row-local control portion and by spaces between said at least two image sensor areas.

13. (previously presented) A CMOS image sensor circuit, comprising:

a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and image sensor logic on said substrate, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually, said image sensor portion having a first area and a second area;

said first CMOS image sensor substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge;

said first CMOS image sensor substrate extending between said first edge, said second edge, and said third edge, such that said first area of said image sensor portion is adjacent said first edge and said third edge of said image sensor substrate

and said second area of said image sensor portion is adjacent said second edge and said third edge of said first CMOS image sensor substrate;

E1 cont

said row logic being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion;

a pixel interpolator and said chip driver circuitry located between said first portion and said second portion of said image sensor portion and said fourth edge of said image sensor substrate; and

a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate.

Claims 14-16. (canceled)

17. (currently amended) A method of fabricating a CMOS imager comprising fabricating at least two CMOS image sensors having an image sensor portion arranged in an array of rows and columns, each of said at least two CMOS image sensors formed to have at least a first set of parallel edges including a first edge and a second edge, said a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge, each of said at least two image sensors having a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor and thereby forming at least two <u>active</u> image sensor areas in each of said at least two CMOS image sensors, said control portion including a pixel

interpolator located between said at least two image sensor areas and one of said edges of said image sensor.

E1 cont'd

18. (original) The method according to claim 17, further comprising:

abutting said at least two CMOS image sensors together; and

integrating said control portions of said at least two CMOS image sensors such that said at least two CMOS image sensors function as a single CMOS imager.

19. (previously presented) A circuit as in claim 1 wherein said row logic masks two columns of the array forming the image sensor portion.

20. (previously presented) A circuit as in claim 1 wherein said row logic is non-photosensitive.

21. (previously presented) A circuit as in claim 1 wherein at least a portion of said row logic divides said image portion into said first and second areas.

22. (previously presented) The CMOS imager according to claim 10, wherein the first and second CMOS image sensors are co-planar.